

# ΕΝΣΩΜΑΤΩΜΕΝΑ ΣΥΣΤΗΜΑΤΑ



**ΤΕΙ ΗΠΕΙΡΟΥ-  
ΣΤΕΦ  
ΤΜΗΜΑ ΜΗΧ. ΠΛΗΡΟΦΟΡΙΚΗΣ Τ.Ε.**

1

Εξάμηνο Διδασκαλίας: 7<sup>ο</sup>

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# ΔΙΑΘΡΩΣΗ ΜΑΘΗΜΑΤΟΣ

- Διαλέξεις αρχιτεκτονικής υπολ. συστημάτων
  - με έμφαση στα ενσωματωμένα δικτυακά συστήματα
- Διαλέξεις προγραμματισμού ενσωματωμένων συστημάτων
- Ειδικά θέματα μικροελεγκτών αισθητήρων
  - Έμφαση στο TI MSP430 / MSP432
- Ασκήσεις και παραδείγματα προγραμματισμού ενσωματωμένων συστημάτων
- Ανάθεση εργασίας ανάπτυξης εφαρμογής



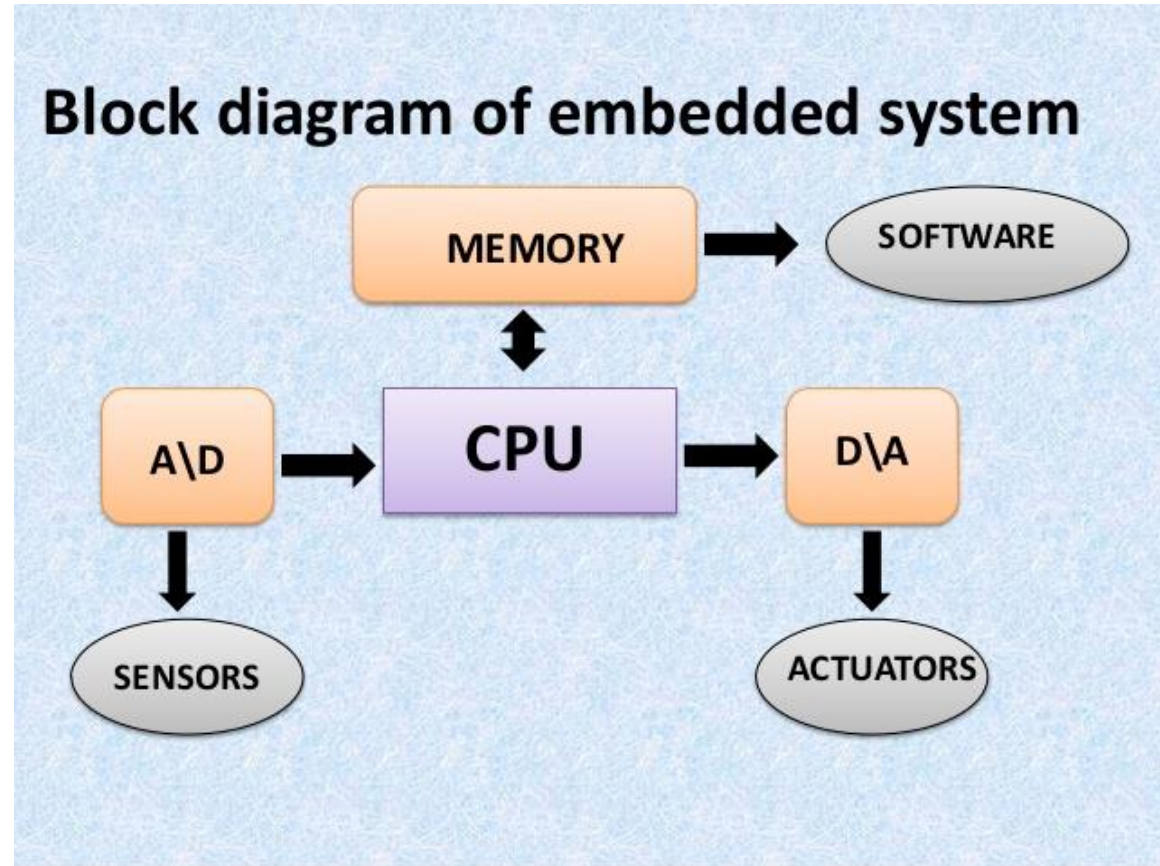
# ΒΑΣΙΚΕΣ ΠΡΟΔΙΑΓΡΑΦΕΣ – ΣΧΕΔΙΑΣΤΗΣ

- FUNCTION (dedicated system) – Systems Eng.
- Form factor – Area - H/W Eng. ( EE +ME)
- Portability –H/W Eng.
- Cost - H/W Eng. + Production Eng.
- Low Power (Battery Life) (H/W + S/W Eng.)
- Response Time -- Real Time Systems (S/W Eng.)
  
- Fault Tolerance (S/W + H/W Eng.)



# ΑΡΧΙΤΕΚΤΟΝΙΚΗ

- Block diagram (H/W – S/W)



<http://www.slideshare.net/apurvazope/introduction-to-embedded-systems-59534882>



# ΣΥΣΤΑΤΙΚΑ

## ○ Απαραίτητα:

- Microprocessor / DSP
- Memory (On-chip and Off chip)
- Communication path with the interacting environment

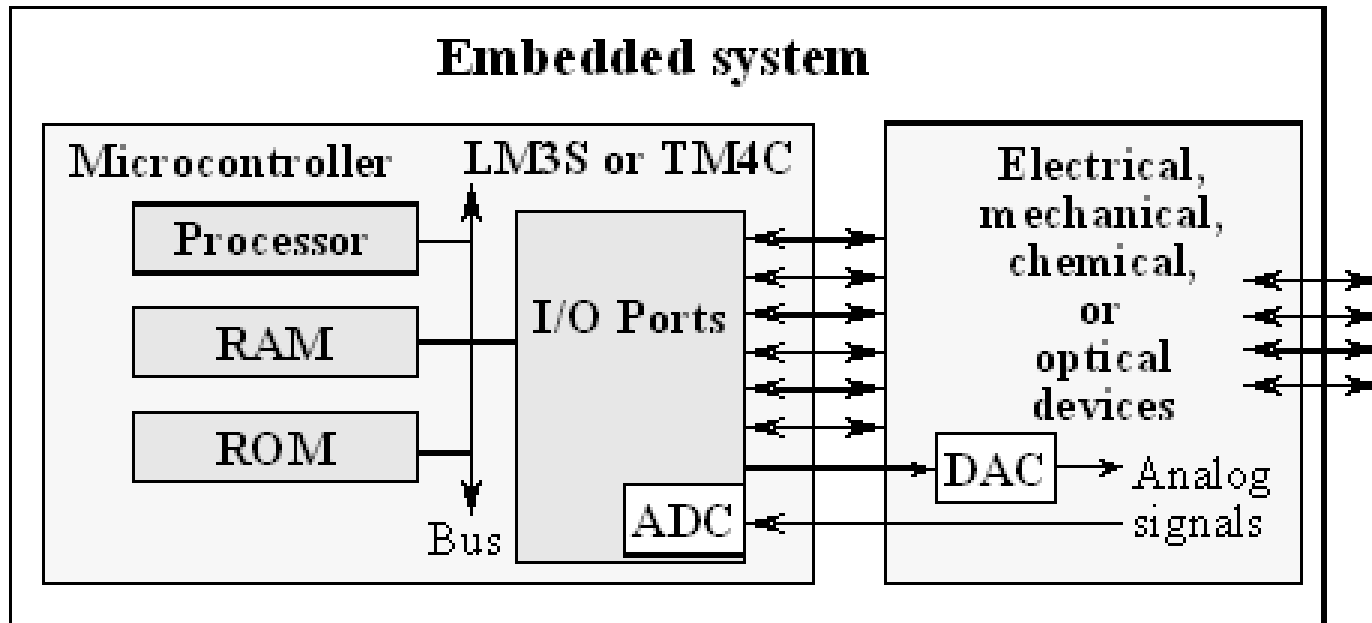
## ○ Προαιρετικά:

- Storage (permanent memory)
- User Interface
- Sensors
- Converters (A-D and D-A)
- Actuators



# ΑΡΧΙΤΕΚΤΟΝΙΚΗ - ΙΙ

- Block diagram
- Έμφαση στην αλληλεπίδραση (I/O)
- Bus?

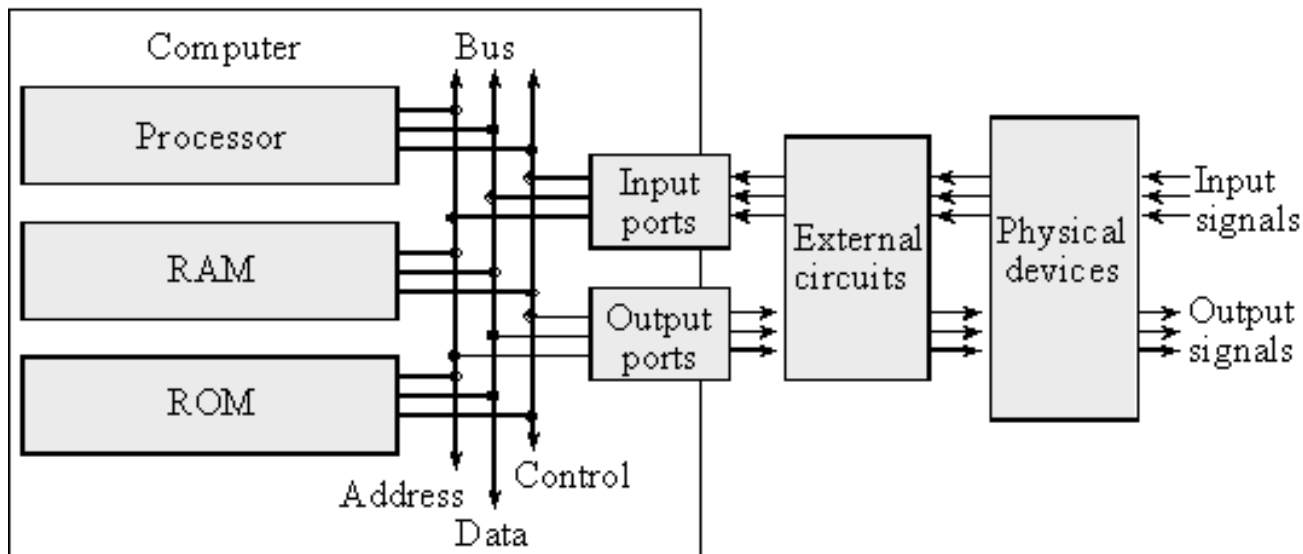


[http://users.ece.utexas.edu/~valvano/Volume1/E-Book/C2\\_FundamentalConcepts.htm](http://users.ece.utexas.edu/~valvano/Volume1/E-Book/C2_FundamentalConcepts.htm)



# ΑΡΧΙΤΕΚΤΟΝΙΚΗ - ΔΙΑΔΡΟΜΟΙ

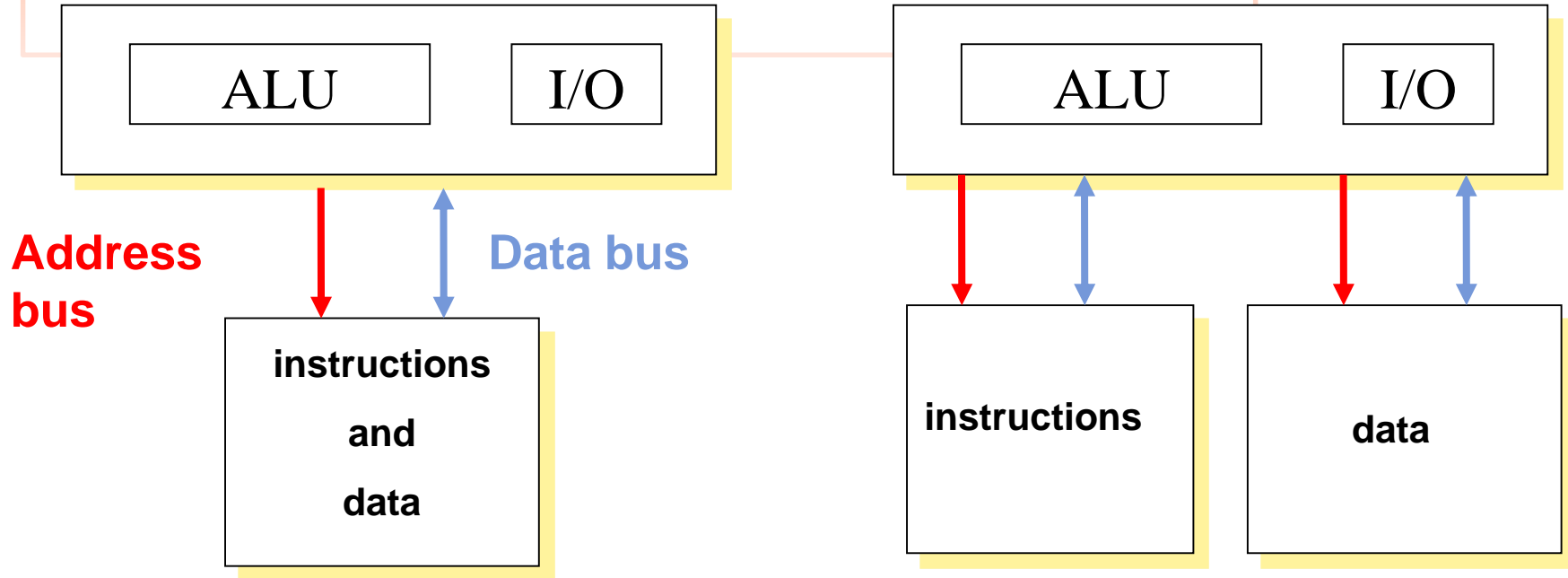
- Bus = Ψηφιακή (παράλληλη) επικοινωνία
- Σύμπλεγμα ψηφιακών αγωγών (διάδρομος δεδομένων)
- Μεταφέρει μονάδες πληροφορίας (bytes, words,...)
- Ελέγχεται από (και συνδέει) μικροεπεξεργαστή ή/και DMA



[http://users.ece.utexas.edu/~valvano/Volume1/E-Book/C2\\_FundamentalConcepts.htm](http://users.ece.utexas.edu/~valvano/Volume1/E-Book/C2_FundamentalConcepts.htm)



# ΜΙΚΡΟΕΠΕΞΕΡΓΑΣΤΕΣ



## Von Neuman architecture

**Area efficient** but requires higher bus bandwidth because instructions and data must compete for memory.

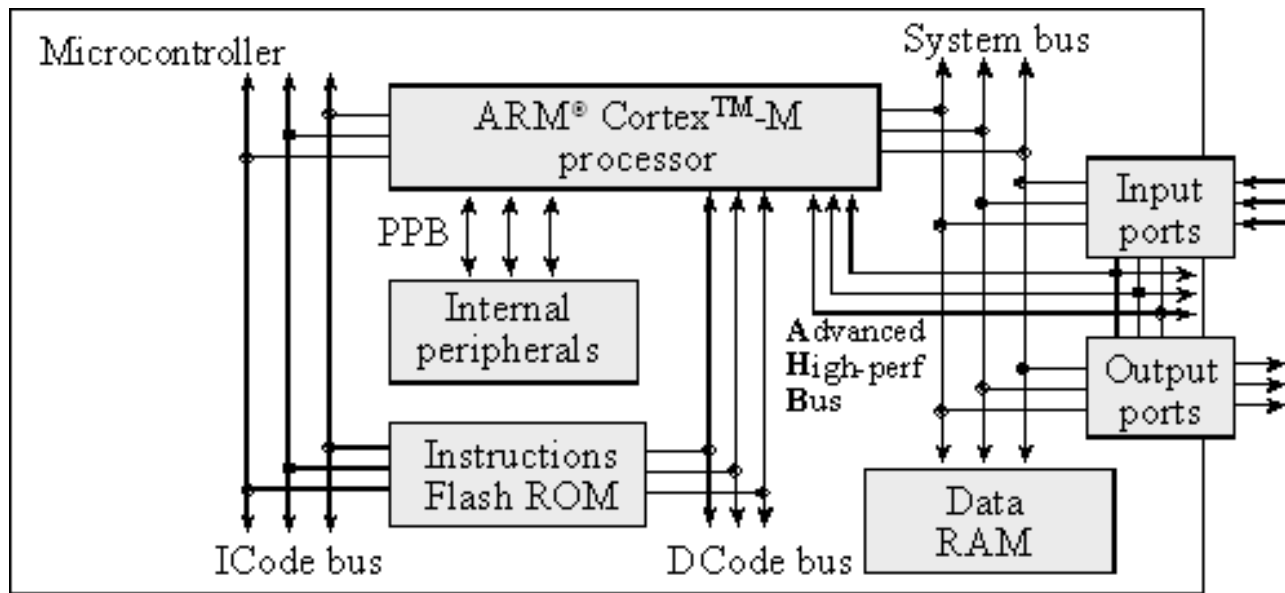
Harvard architecture was coined to describe machines with separate memories.

**Speed efficient:** Increased parallelism.



# ADVANCED HARVARD (ARM CORTEX)

- Διαχωρισμός I- και D- διαδρόμων από τον διάδρομο συστήματος
- Διαχωρισμός των ροών προγράμματος και (εξωτερικών) δεδομένων

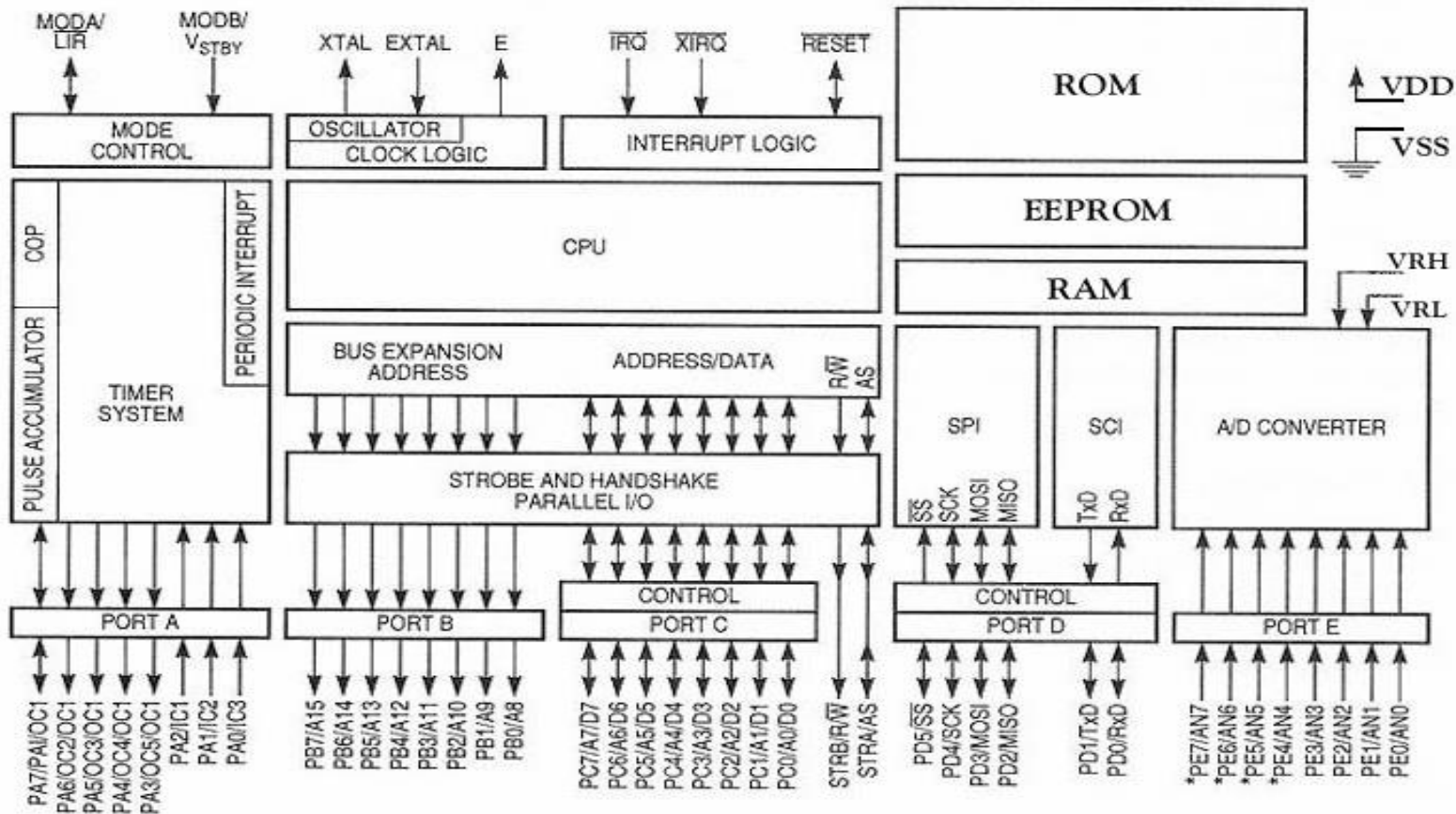


# ΜΙΚΡΟΕΛΕΓΚΤΕΣ

- A highly integrated microprocessor designed specifically for use in embedded systems. Microcontrollers typically include:
  - an integrated CPU
  - memory (RAM + ROM / EPROM / EEPROM)
  - input / output devices
    - ADC (Analog-to-digital) converters
    - DAC (Digital-to-analog) converters
    - UARTs (Universal Asynchronous Receiver Transmitter)
    - I<sup>2</sup>C (Inter-Integrated Circuit)
  - Accelerators (video, encryption)



# ΜΙΚΡΟΕΛΕΓΚΤΕΣ



\* NOT BONDED ON 48-PIN VERSION.



## MICROCONTROLLER CHARACTERISTICS

- Integration: Able to implement a whole design onto a single chip.
- Cost: Are usually low-cost devices (a few \$ each);
- Clock frequency: Compared with other devices (microprocessors and DSPs), MCUs use a low clock frequency:
  - MCUs today run up to 100 MHz/100 MIPS (Million Instructions Per Second).
- Power consumption: Low power (battery operation);
- Bits: 4 bits (older devices) to 32 bits devices;
- Memory: Limited available memory, usually less than 1 MByte;
- Input/Output (I/O): Low to high pin-out count (8 to 150) .

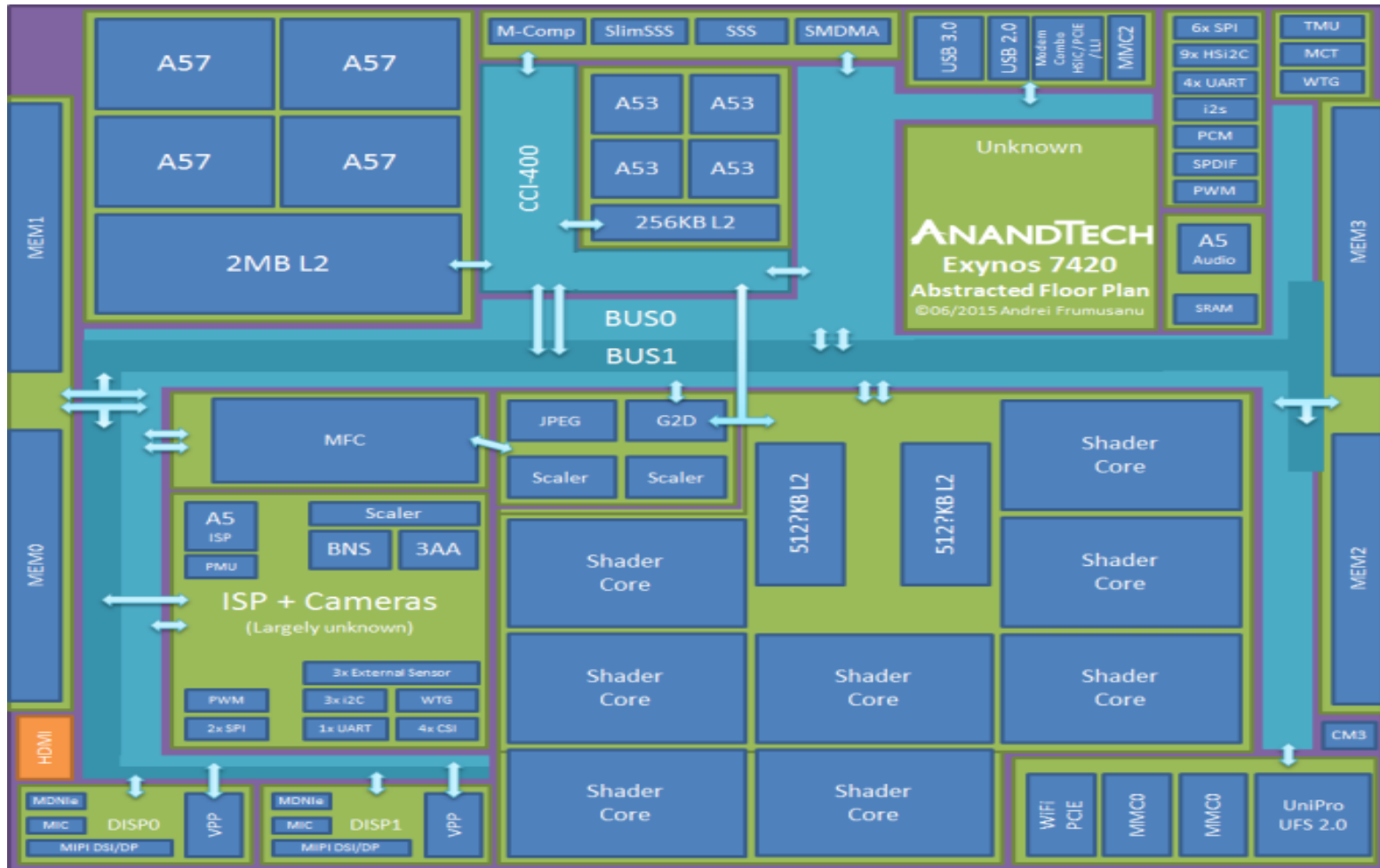


## HIGH END MICROCONTROLLERS - SoCs

- Integration: Many processors (cores) and accelerators on chip.
- Cost: Significantly higher than  $\mu$ Cs;
- Clock frequency: High, typically  $> 1\text{GHz}$
- Power: Very high compared to  $\mu$ Cs; advanced power management
  - Voltage islands
  - Clock scaling / voltage scaling (from 0,5V to 1,8V)
- On chip video/LCD driver and more
  
- From the SW point of view: **NO DIFFERENCE** between a big SoC and a (respectively) complex motherboard
- **EXCEPT:** for debugging /SW verification

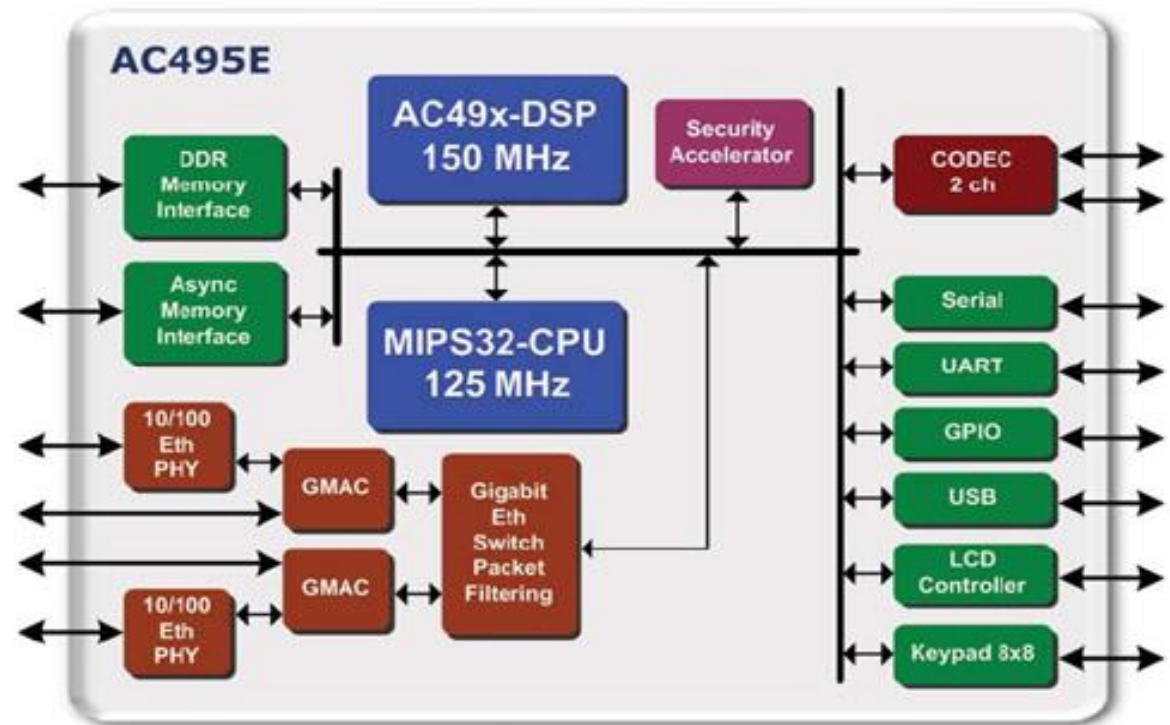


# SoC EXAMPLE



# APPLICATION SPECIFIC ICs (ASSP)

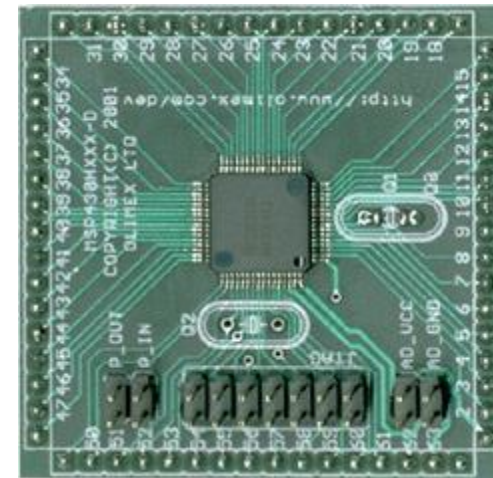
- Integration: Between  $\mu$ Cs and SoCs.
- Clock frequency: High, typically  $>200\text{MHz}$
- Serves a specific kind of applications
- Example: IP phone codec (can be also stand-alone phone)



Microcontrollers (MCU)				Application (MPU)		
<b>MSP430</b>	<b>C2000</b>	<b>Tiva C</b>	<b>Hercules</b>	<b>Sitara</b>	<b>DSP</b>	<b>Keystone</b>
16-bit	32-bit	32-bit	32-bit	32-bit	16/32-bit	32-bit
<b>Ultra Low Power &amp; Cost</b>	<b>Real-time</b>	<b>All-around MCU</b>	<b>Safety</b>	<b>Linux Android</b>	<b>All-around DSP</b>	<b>Massive Performance</b>
<b>MSP430 ULP RISC MCU</b>	<ul style="list-style-type: none"> <li>Real-time C28x MCU</li> <li>ARM M3+C28</li> </ul>	<b>ARM Cortex-M4F</b>	<ul style="list-style-type: none"> <li>ARM Cortex-M3</li> <li>Cortex-R4</li> </ul>	<ul style="list-style-type: none"> <li>ARM Cortex-A8</li> <li>Cortex-A9</li> </ul>	<ul style="list-style-type: none"> <li>DSP C5000</li> <li>C6000</li> </ul>	<ul style="list-style-type: none"> <li>C66 + C66</li> <li>A15 + C66</li> <li>A8 + C64</li> <li>ARM9 + C674</li> </ul>
<ul style="list-style-type: none"> <li>Low Pwr Mode <ul style="list-style-type: none"> <li>250nA (RTC)</li> <li>770nA (LCD)</li> </ul> </li> <li>Analog I/F</li> <li>USB and RF</li> </ul>	<ul style="list-style-type: none"> <li>Motor Control</li> <li>Digital Power</li> <li>Precision Timers/PWM</li> </ul>	<ul style="list-style-type: none"> <li>32-bit Float</li> <li>Nested Vector IntCtrl (NVIC)</li> <li>Ethernet (MAC+PHY)</li> </ul>	<ul style="list-style-type: none"> <li>Lock step Dual-core R4</li> <li>ECC Memory</li> <li>SIL3 Certified</li> </ul>	<ul style="list-style-type: none"> <li>\$5 Linux CPU</li> <li>3D Graphics</li> <li>PRU-ICSS industrial subsys</li> </ul>	<ul style="list-style-type: none"> <li>C5000 Low Power DSP</li> <li>32-bit fix/float C6000 DSP</li> </ul>	<ul style="list-style-type: none"> <li>Fix or Float</li> <li>Up to 12 cores 4 A15 + 8 C66x</li> <li>DSP MMAC's: 352,000</li> </ul>
<b>TI-RTOS</b>	<b>TI-RTOS (k)</b>	<b>TI-RTOS</b>	<b>3<sup>rd</sup> Party (only)</b>	<b>Linux, Android, TI-RTOS Kernel</b>	<b>C5x: DSP/BIOS</b> <b>C6x: TI-RTOS (k)</b>	<b>Linux TI-RTOS (k)</b>
Flash: 512K FRAM: 128K	512K Flash	1MB Flash	256K to 3M Flash	L1: 32K x 2 L2: 256K	L1: 32K x 2 L2: 256K	L1: 32K x 2 L2: 1M + 4M
25 MHz	300 MHz	120 MHz	220 MHz	1.35 GHz	800 MHz	1.4 GHz
\$0.25 to \$9.00	\$1.85 to \$20.00	\$1.00 to \$8.00	\$5.00 to \$30.00	\$5.00 to \$25.00	\$2.00 to \$25.00	\$30.00 to \$225.00

# ΧΑΡΑΚΤΗΡΙΣΤΙΚΑ MSP430

- Ultralow-power architecture
  - 0.1- $\mu$ A RAM retention, 0.8- $\mu$ A real-time clock mode
  - 250- $\mu$ A / MIPS active
- 16-bit RISC CPU
  - 27 instructions and 7 addressing modes
- von-Neumann architecture has one address space shared with
  - special function registers (SFRs)
  - peripherals
  - RAM (128 bytes  $\rightarrow$  2k)
  - Flash / ROM (1k  $\rightarrow$  60k)
- In-system programmable Flash
- Analog
  - 12-bit or 10-bit ADC, 12-bit dual-DAC
- USART Peripheral Interface
- Digital I/O ports
  - Two, Three or Six 8-bit I/O ports



# RESOURCES

- [www.ti.com/msp430](http://www.ti.com/msp430)



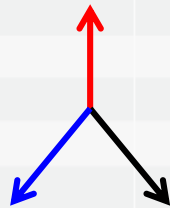
# MSP430 Families

Series	Ultra-Low Power				FRxx FRAM	Low Power + Performance	Security + Communications	
	L09x Low Voltage	G2x/I2x	F1x	F2x/F4x			RF-430	CC430
Part Number								
Max speed (MHz)	4	16	16	16	24	25	4	20
NVM (max KB)	0	56	120	120	128	512	ROM Fixed Function	32
SRAM (max KB)	2	4	10	8	2	67	4	4
GPIO	11	4-32	10-48	14-80	17-40	29-90	Up to 8	30-44
Comparator	•	•	•	•	•	•	•	•
Timer	•	•	•	•	•	•	•	•
ADC	•	•	•	•	•	•	On select	•
DAC	•		•	•		•		
UART		•	•	•	•	•	•	•
I <sup>2</sup> C		•	•	•	•	•	•	•
SPI		•	•	•	•	•	•	•
Capacitive touch		•			•			
Multiplier		•	•	•	•	•		•
DMA			•	•	•	•		•
Op amps			•	•				
LCD				•	•	•		•
RTC				•	•	•		•
PMM					•	•	•	•
1.8-V I/O						•		
CRC					•	•	•	•
High-resolution timer						•		
USB						•		
Hardware encryption (AES)					•	•		•
FRAM					•		On select	
RF							13.56 MHz (ISO 15693 or ISO 14443B interface)	Sub-1GHz

Low Power +  
Performance

Ultra Low  
Power

Security +  
Comm



# FRAM MCU DELIVERS MAX BENEFITS

	FRAM	SRAM	EEPROM	Flash
<b>Non-volatile</b> Retains data without power	<b>Yes</b>	<b>No</b>	<b>Yes</b>	<b>Yes</b>
<b>Write speeds</b>	<b>10 ms</b>	<b>&lt;10 ms</b>	<b>2 secs</b>	<b>1 sec</b>
<b>Average active Power</b> ( $\mu A/MHz$ )	<b>110</b>	<b>&lt;60</b>	<b>50mA+</b>	<b>230</b>
<b>Write endurance</b>	<b><math>10^{15}</math></b>	<b>Unlimited</b>	<b>100,000</b>	<b>10,000</b>
<b>Dynamic</b> Bit-wise programmable	<b>Yes</b>	<b>Yes</b>	<b>No</b>	<b>No</b>
<b>Unified memory</b> Flexible code/data partitioning	<b>Yes</b>	<b>No</b>	<b>No</b>	<b>No</b>



# F5xx Key Features

## Ultra-Low Power

- ◆ 160  $\mu$ A/MIPS
- ◆ 2.5  $\mu$ A standby mode
- ◆ Integrated LDO, BOR, WDT+, RTC
- ◆ 12 MHz @ 1.8V
- ◆ Wake up from standby in  $<5 \mu$ s

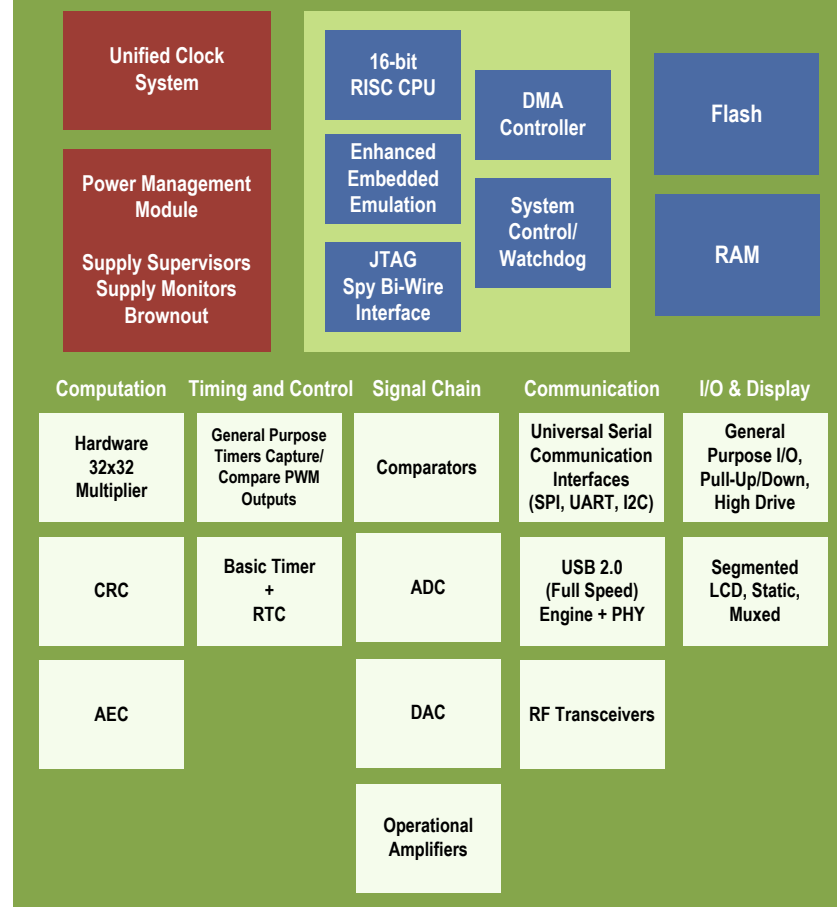
## Increased Performance

- ◆ Up to 25 MHz
- ◆ 1.8V ISP Flash erase and write
- ◆ Fail-safe, flexible clocking system
- ◆ User-defined Bootstrap Loader
- ◆ Up to 1MB linear memory addressing

## Innovative Features

- ◆ Multi-channel DMA supports data movement in standby mode
- ◆ Industry leading code density
- ◆ More design options including USB, RF, encryption, LCD interface

## MSP430F5xx Block Diagram



Looking at the 'FR59xx...

## ΑΠΑΙΤΥΕΙΑΚΟ ΣΥΣΤΗΜΑ: MSP432 LAUNCHPAD (1/3)

- USB-based MSP430 development tool to evaluate the MSP432 microcontroller;
- The MSP432P401R LaunchPad features the MSP432P401R low power microcontroller – which includes a 48MHz ARM Cortex M4F
- It includes an on-board emulator with EnergyTrace+ Technology
  - You can program and debug your projects through CCS and USB,
  - while also measuring total system energy consumption



## ΑΠΑΙΤΥΕΙΑΚΟ ΣΥΣΤΗΜΑ: MSP432 LAUNCHPAD (2/3)

- MSP432 features and integrated peripherals:
  - 48MHz 32-bit ARM Cortex M4F with Floating Point Unit and DSP acceleration
  - Power consumption: 95uA/MHz active, and 850nA RTC standby operation
  - Analog: 24Ch 14-bit differential 1MSPS SAR ADC, Two Comparators
  - Digital: Advanced Encryption Standard (AES256) Accelerator, CRC, DMA, HW MPY32
  - Memory: 256KB Flash, 64KB RAM
  - Timers: 4 x16-bit, and 2 x 32-bit
  - Communication: Up to 4 I2C, 8 SPI, 4 UART



## ΑΠΑΙΤΥΕΙΑΚΟ ΣΥΣΤΗΜΑ: MSP432 LAUNCHPAD (3/3)

- Board features:
  - Highly integrated, ultra-low-power MSP432 MCU;
  - 40 pin BoosterPack Connector, and support for 20 pin BoosterPacks
  - Onboard XDS-110ET emulator featuring EnergyTrace+ Technology
  - Back-channel UART via USB to PC
  - 2 LEDs for visual feedback;
  - 2 Interruptible push buttons for user feedback.

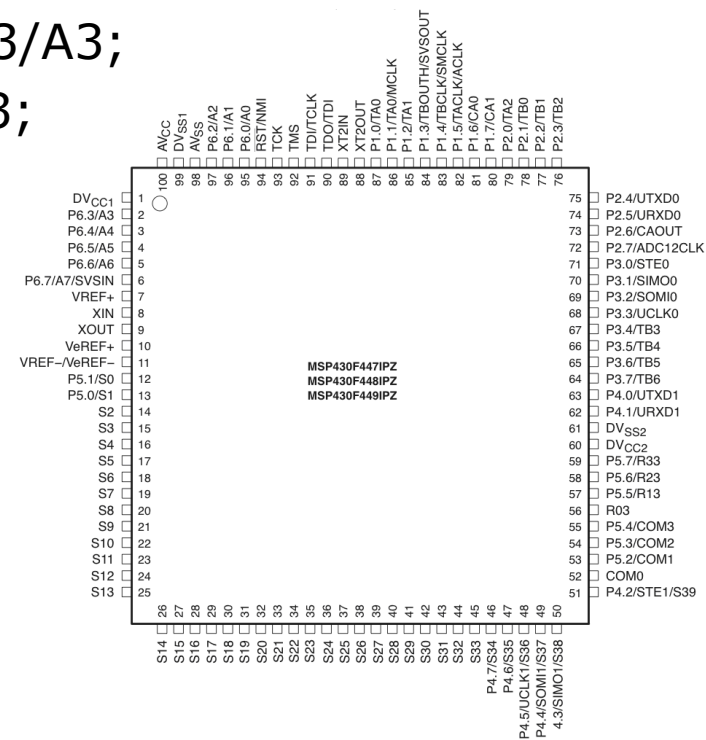


- ❑ Οι κατασκευαστές ηλεκτρονικών εξαρτημάτων παρέχουν φυλλάδια δεδομένων που περιέχουν προδιαγραφές και περιγράφουν τα χαρακτηριστικά τους.
  
- ❑ Τα φυλλάδια δεδομένων δίνουν τα ηλεκτρικά χαρακτηριστικά της διάταξης και τις λειτουργίες των ακροδεκτών (pins), χωρίς όμως να περιγράφουν λεπτομερειακά την εσωτερική λειτουργία τους.
  
- ❑ Για τις πιο πολύπλοκες διατάξεις παρέχονται τεχνικά έγγραφα που βοηθούν στην ανάπτυξη εφαρμογών, όπως:
  - Σημειώσεις Εφαρμογών;
  - Οδηγούς Χρηστών;
  - Οδηγούς Σχεδιαστών;
  - Πακέτα σχεδίων, κτλ...

- ❑ **Τα φυλλάδια δεδομένων περιλαμβάνουν πληροφορίες:**
  - Σχετικά με την χαρακτηριστική αρίθμηση της διάταξης ή της σειράς της διάταξης.
  - Ηλεκτρικά χαρακτηριστικά:
    - Μέγιστη και ελάχιστη τάση λειτουργίας
    - Εύρος θερμοκρασίας χρήσης π.χ. 0 έως 70 βαθμούς C
    - Η δυνατότητα οδήγησης για κάθε ακροδέκτη εξόδου, όπως επίσης το συνολικό όριο του ολοκληρωμένου.
    - Συχνότητες Ρολογιού
    - Τα ηλεκτρικά χαρακτηριστικά των ακροδεκτών (χωρητικότητα, αγωγιμότητα, αντίσταση)
    - Ανοχή θορύβου ή ο θόρυβος που παράγεται από την ίδια την διάταξη.
    - Φυσικές ανοχές...

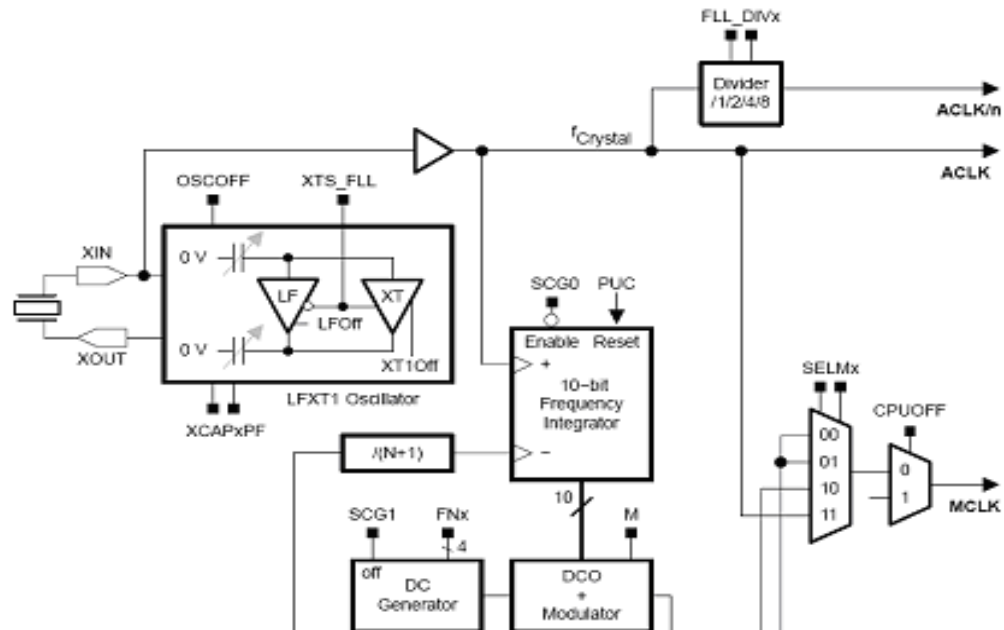
## ❑ Φυλλάδια δεδομένων του MSP430:

- Η διάταξη έχει ένα μεγάλο αριθμό περιφερειακών
- Κάθε ακροδέκτης εισόδου/εξόδου συνήθως έχει πάνω από μία λειτουργία;
- Περιλαμβάνει πίνακα περιγραφής της λειτουργίας κάθε ακροδέκτη
- Παράδειγμα, Αριθμός ακροδέκτη 2 = P6.3/A3;
  - Ψηφιακή θύρα 6 εισόδου/εξόδου bit 3;
  - 3<sup>η</sup> αναλογική είσοδος.



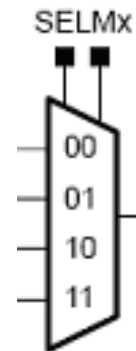
## ❑ Οδηγός χρήστη MSP430 :

- Τα περισσότερα περιφερειακά αναπαρίστανται με Δομικά Διαγράμματα.
- Παράδειγμα: Μέρος του τμήματος του δομικού διαγράμματος ρολογιού του MSP430F44x :



## ❑ Οδηγός Χρήστη MSP430:

- Παράδειγμα: Δομικό Διάγραμμα Μέρος τμήματος ρολογιού του MSP430F44x: Λεπτομέρεια SELMx;
- Πολυπλεξία: (4 είσοδοι σε 1 έξοδο):
  - SELMx = 00: Η έξοδος δρομολογείται στην 1η έξοδο του πολυπλέκτη
  - SELMx = 01: Η έξοδος δρομολογείται στην 2η έξοδο του πολυπλέκτη και αυτό συνεχίζεται..
  - SELMx είναι μια μνημονική λέξη 2-bit: SELM1 (MSB), SELM0 (LSB).
- Για να χρησιμοποιηθεί το περιφερειακό, είναι αναγκαίο να διαμορφωθούν οι καταχωρητές:
  - SELMx βρίσκεται στον FLL\_CTL1 καταχωρητή.



## ❑ Οδηγός χρήστη (User's Guide) του MSP430 :

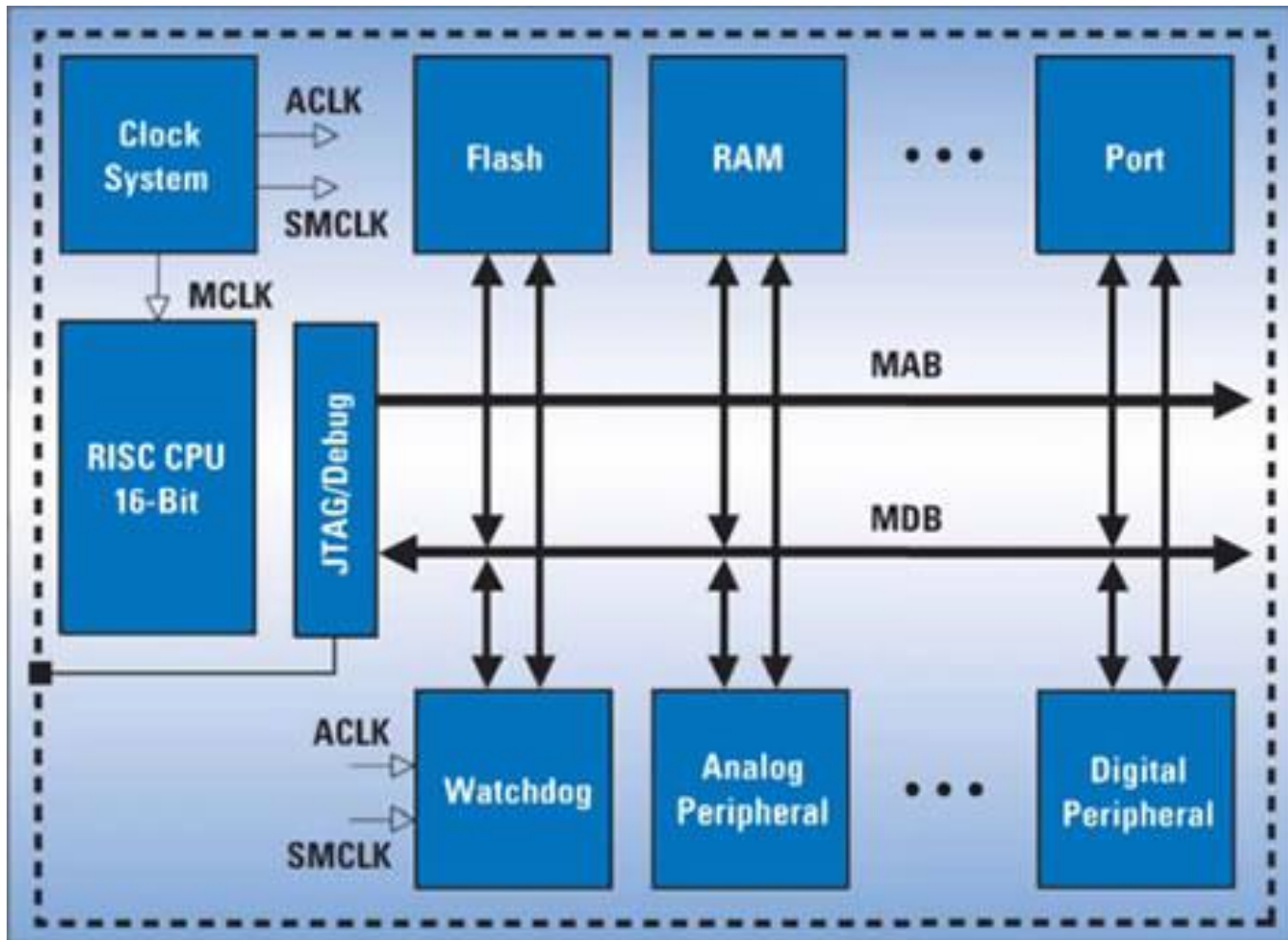
- SELM<sub>x</sub> είναι το 3<sup>ο</sup> και 4<sup>ο</sup> bit του FLL\_CTL1 καταχωρητή ελέγχου.

### FLL\_CTL1, FLL+ control register 1

7	6	5	4	3	2	1	0	
-	SMCLKOFF	XT2OFF	SELM <sub>x</sub>		SELS	FLL_DIV <sub>x</sub>		
Bit	Description							
6	SMCLKOFF	Disable the submain clock signal (SMCLK):						
		SMCLKOFF = 0	⇒		SMCLK active			
		SMCLKOFF = 1	⇒		SMCLK inactive			
5	XT2OFF	Disable the second crystal oscillator (XT2):						
		XT2OFF = 0	⇒		XT2 active			
		XT2OFF = 1	⇒		XT2 inactive			
4-3	SELM <sub>x</sub>	Select the master clock (MCLK) source:						
		SELM1 SELM0 = 0 0	⇒		DCO			
		SELM1 SELM0 = 0 1	⇒		DCO			
		SELM1 SELM0 = 1 0	⇒		XT2			
		SELM1 SELM0 = 1 1	⇒		LFXT1			
2	SELS	Select the submain clock (SMCLK) source:						
		SELS = 0	⇒		DCO			
		SELS = 1	⇒		XT2			
1-0	FLL_DIV <sub>x</sub>	Select the auxiliary clock (ACLK) signal divider:						
		FLL_DIV_0 = 0 0	⇒		Divider factor: /1			
		FLL_DIV_1 = 0 1	⇒		Divider factor: /2			
		FLL_DIV_2 = 1 0	⇒		Divider factor: /4			
		FLL_DIV_3 = 1 1	⇒		Divider factor: /8			

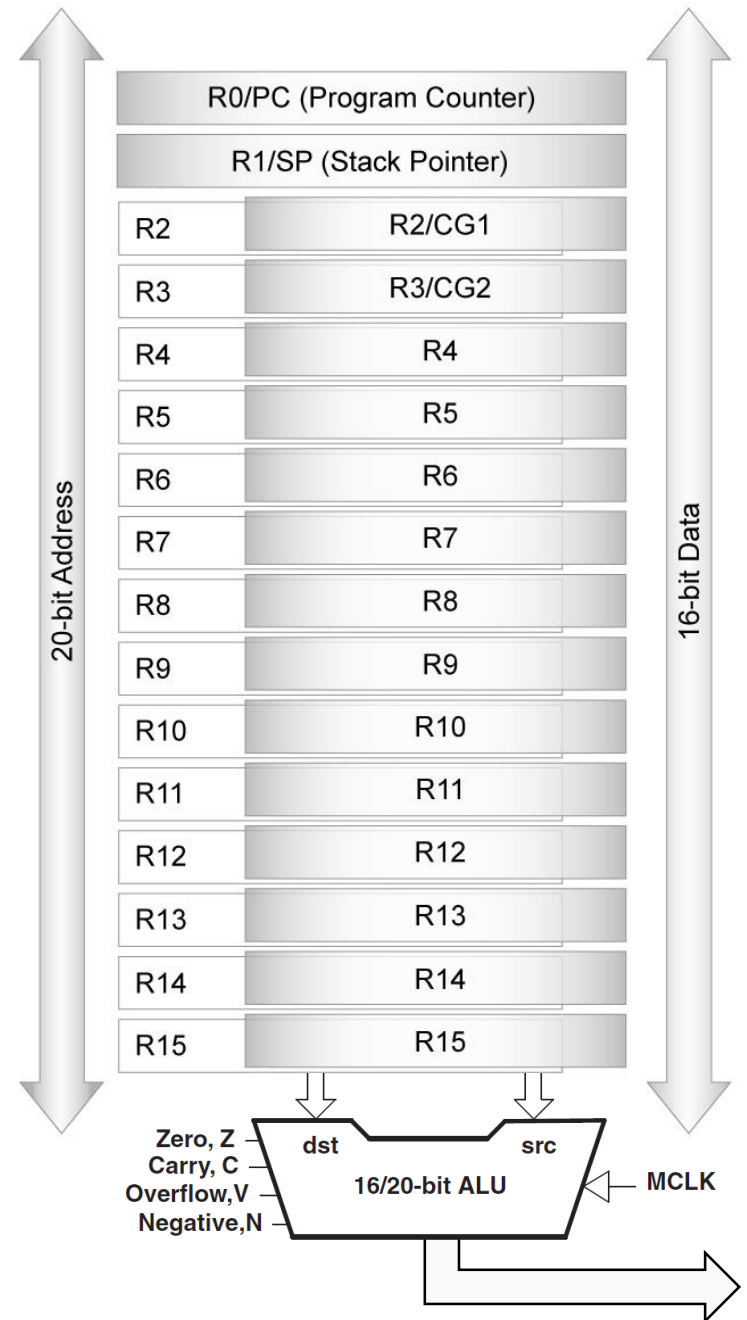
# MSP430 ARCHITECTURE

- Block diagram:



# MSP430 CPU

- ◆ **Efficient, ultra-low power CPU**
- ◆ **C-compiler friendly**
- ◆ **RISC architecture**
  - ◆ 51 instructions
  - ◆ 7 addressing modes
  - ◆ Constant generator
- ◆ **Single-cycle register operations**
- ◆ **Bit, byte and word processing**
- ◆ **1MB unified memory map**
  - ◆ No paging
- ◆ **Extended addressing modes**
  - ◆ Page-free 20-bit reach
  - ◆ Improved code density
  - ◆ Faster execution
- ◆ **100% code compatible with earlier versions**



# Unified Memory Map

## In-System Prog (ISP)

- ♦ Write using: User program, JTAG, BSL
- ♦ Byte, word, long-word
- ♦ Erase one (or all) segments at a time

## Main Flash

- ♦ 512 byte segments
- ♦ Start address moves according to RAM

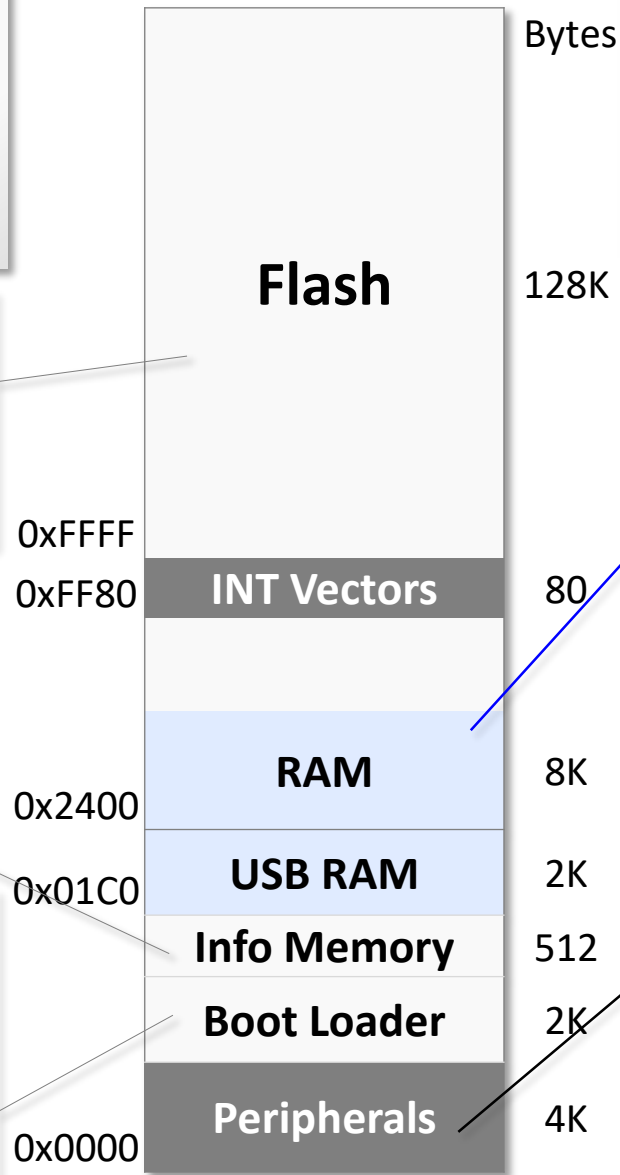
## Info Memory

- ♦ Use for your own calibration data, etc.
- ♦ 4 segments (A-D)
- ♦ 128 byte segments

## Boot Loader (BSL)

- ♦ Program Flash/RAM with serial (slau319)
- ♦ Password protected
- ♦ 512 byte segments

## 'F5529 Memory Map



## MSP430 Memory

- ♦ Unified memory map (program or data)
- ♦ Absolutely no paging

## RAM

- ♦ Always a contig. block
- ♦ If enabled, USB port uses first 2K
- ♦ RAM segments can be powered down

## Device Descriptors (TLV)

- ♦ Factory calibration data, periph support,...
- ♦ Found in peripherals (at 0x1A00)

# ADDRESS SPACE

- Mapped into a single, contiguous address space:
  - All memory, including RAM, Flash/ROM, information memory, special function registers (SFRs), and peripheral registers.

- **Memory Map:**

Memory Address	Description	Access
End: 0FFFFh	<b>Interrupt Vector Table</b>	Word/Byte
Start: 0FFE0h		
End: 0FFDFh	<b>Flash/ROM</b>	Word/Byte
Start *: 0F800h 01100h		
End *: 010FFh	<b>Information Memory (Flash devices only)</b>	Word/Byte
0107Fh		
Start: 01000h	<b>Boot Memory (Flash devices only)</b>	Word/Byte
End: 0FFFh		
Start: 0C00h	<b>RAM</b>	Word/Byte
End *: 09FFh		
027Fh	<b>16-bit Peripheral modules</b>	Word
Start: 0200h		
End: 01FFh	<b>8-bit Peripheral modules</b>	Byte
Start: 0100h		
End: 00FFh	<b>Special Function Registers</b>	Byte
Start: 0010h		
End: 000Fh		
Start: 0000h		



# INTERRUPT VECTOR TABLE

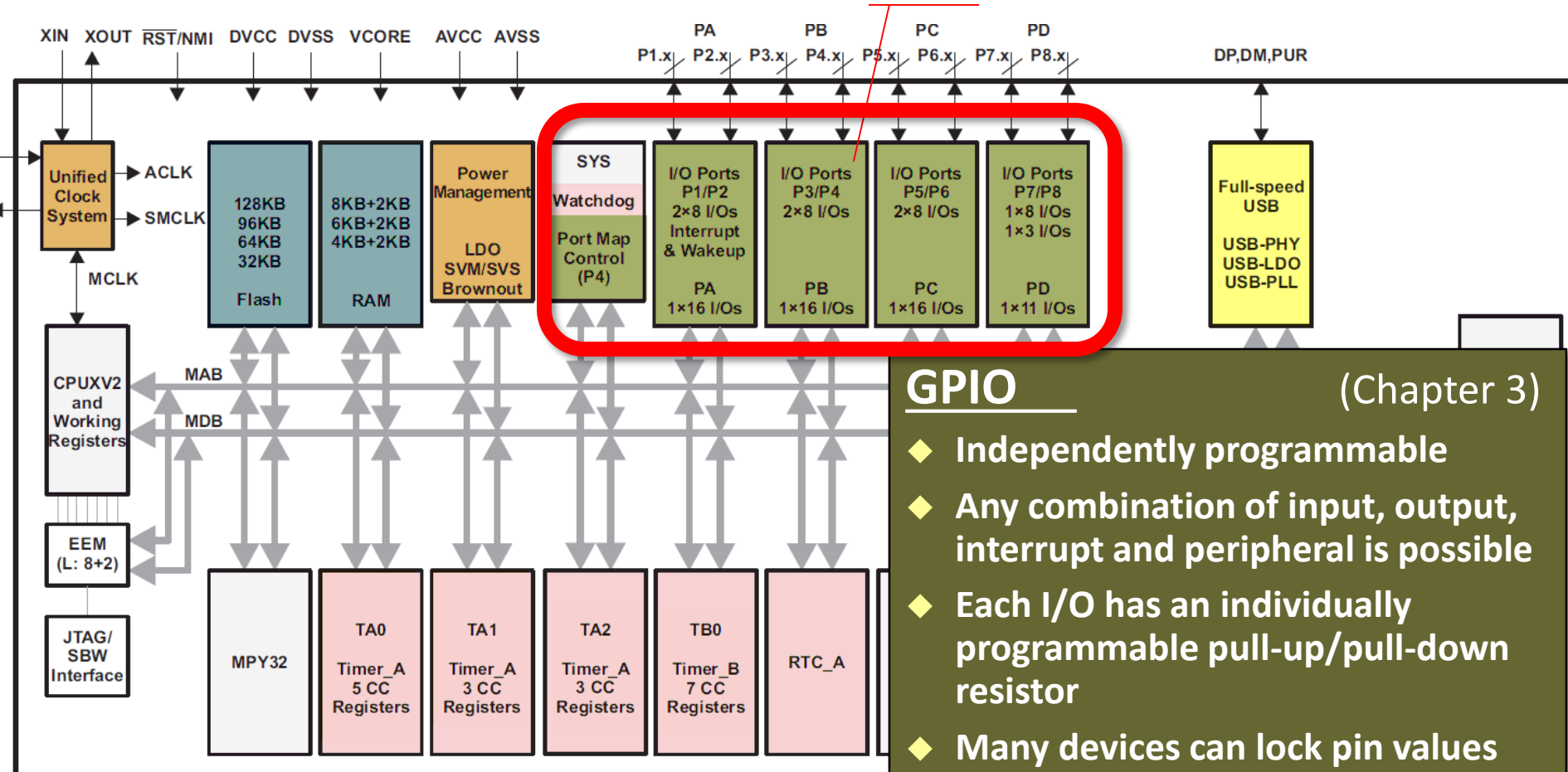
- Mapped at the very end of memory space (upper 16 words of Flash/ROM):  
0xFFE0h - 0xFFFEh (4xx devices);
- Priority of the interrupt vector increases with the word address.

Vector Address	Priority	'2xx	'4xx
0xFFFE	31, Highest	Hard Reset/ Watchdog	Hard Reset/ Watchdog
0xFFFC	30	Oscillator/ Flash/NMI	Oscillator/ Flash/NMI
0xFFFA	29	Timer_B (22x2, 22x4, 23x, 24x, 26x)	Timer_B ('43x and'44x)
0xFFF8	28	Timer_B (22x2, 22x4, 23x, 24x)	Timer_B ('43x and'44x)
0xFFF6	27	Comparator_A+ (20x1, 21x1, 23x, 24x, 26x)	Comparator
0xFFF4	26	Watchdog Timer+	Watchdog Timer
0xFFF2	25	Timer_A	USART0 Rx ('43x and'44x)
0xFFF0	24	Timer_A	USART0 Tx ('43x and'44x)
0xFFEE	23	USCI Rx (22x2, 22x4, 23x, 24x, 26x) I2C status (23x, 24x)	ADC ('43x and'44x)
0xFFEC	22	USCI Tx (22x2, 22x4, 23x, 24x, 26x) I2C Rx/Tx (23x, 24x, 26x)	Timer_A
0xFFEA	21	ADC10 (20x2 22x2, 22x4) ADC12 (23x, 24x, 26x) SD16_A (20x3)	Timer_A
0xFFE8	20	USI (20x2, 20x3)	Port 1
0xFFE6	19	Port P2	USART1 Rx ('44x)
0xFFE4	18	Port P1	USART1 Tx ('44x)
0xFFE2	17	USCI Rx (23x, 24x, 26x) I2C status (241x, 261x)	Port 2
0xFFE0	16	USCI Tx (23x,24x) I2C Rx/Tx (241x, 261x)	Basic Timer
	15	DMA (241x, 261x)	
	14	DAC12 (241x, 261)	
	13 to 0, Lowest	Reserved	



# MSP430 GPIO (Chapter 3)

## GPIO CH 3



'F5529 block diagram

## GPIO

(Chapter 3)

- ◆ Independently programmable
- ◆ Any combination of input, output, interrupt and peripheral is possible
- ◆ Each I/O has an individually programmable pull-up/pull-down resistor
- ◆ Many devices can lock pin values during low-power modes
- ◆ Some devices support touch-sense capability built into the pins

- ❑ **DSP MSP430 devices have up to eight digital I/O ports implemented, P1 to P8. Each port has eight I/O pins.**
- ❑ **Every I/O pin is individually configurable for input or output direction, and each I/O line can be individually read or written to.**
- ❑ **Ports P1 and P2 have interrupt capability.**
- ❑ **The digital I/O features include:**
  - Independently programmable individual I/Os
  - Any combination of input or output
  - Independent input and output data registers
  - Individually configurable pullup or pulldown resistors
- ❑ **On eZ430 board, RED LED is connected to P1.0**



# HELLO WORLD



```
WDTCTL = WDTPW + WDTHOLD;           // Stop watchdog  
timer  
P1DIR |= 0x01;                       // Set P1.0 to output  
direction  
for (;;)                                 
{  
    volatile unsigned int i;          // volatile to prevent optimization  
    P1OUT ^= 0x01;                   // Toggle P1.0 using exclusive-OR  
- Red Blinks  
    i = 10000;                        // SW Delay  
    do i--;  
    while (i != 0);  
}
```

## □ Hello world (LED blink)

### □ Exercises:

- Reduce blink Frequency
- Blink RED/Green (alternating)
- Blink Green twice as fast